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E Sahouria, Y Granik, N Cobb, O Touban - comppub.com

... **optical** and process **simulation** are **Optical Rule Checking** ... image (Figure 4). Conventional DRC **rules** implement these ... A fast **ORC check** then determines which edges ...[View as HTML](#) - [Web Search](#) - [nsti.org](#) - [comppub.com](#) - [nsti.org](#)**Sub-Wavelength Lithography Using OPC**

FM Schellenberg - fabtech.org

... An **ORC check** can describe the magnitude of the problem ... be more broadly used to represent "**optical** and process ... form of simple shape manipu- lation **rules**, or a ...[Web Search](#) - [semiconductorfabtech.com](#) - [eecs.umich.edu](#) - [semiconductorfabtech.com](#)**A Fast Lithography Verification Framework for Litho-Friendly Layout Design**

YC Ban, SH Choi, KH Lee, DH Kim - doi.ieeecomputersociety.org

... To **check** the post-OPC mask data, the litho ... in Figure 6. Here, is the **optical** system wavelength ... OPC works within the constraints of mask manufacturability **rules**. ...[Web Search](#)**Adoption of OPC and the Impact on Design and Layout**

FM Schellenberg, O Touban, L Capodici, B Socha - DAC, 2001 - portal.acm.org

... by changing aperture sizes and shapes (**optical** and process ... designed layout and a DRC **check** of the ... generated, and then checked using conventional design **rules**. ...[Cited by 10](#) - [Web Search](#) - [sigda.org](#) - [hwswworld.com](#) - [videos.dac.com](#) - [all 12 versions »](#)**Detailed Placement for Improved Depth of Focus and CD Control**

P Gupta, AB Kahng, CH Park - Proc. Asia and South Pacific Design Automation Conf., Jan, 2005 - vlsicad.ucsd.edu

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A Reich, R Boone, W Grobman, C Browning - 21 stAnnual BACUS Symposium on Photomask Technology, ..., 2001 - io.com

... different range effects and yield different physical and **optical** responses, so ... Delay Models Topology / **Rules** ... crucial **check** in the case of tiling is to assure ...[Cited by 2](#) - [View as HTML](#) - [Web Search](#) - [si2.org](#) - [adsabs.harvard.edu](#) - [link.aip.org](#) - [all 5 versions »](#)**Estimating the spectral response function of the CASI-2**

KY CHOI, EJ MILTON - eprints.soton.ac.uk

... is reasonable, as there are general **rules** that approximately ... the detector array within

the same **optical** system (pers. ... providing a simple way to **check** for any ...

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### Quantum computation and Shor's factoring algorithm

A Ekert, R Jozsa - Reviews of Modern Physics, 1996 - [link.aps.org](#)

... It followed by a trial division to **check** whether m ... all the amplitudes using the transition **rules** of the ... than the time scale of the **optical** interaction (the ...


[Cited by 477](#) - [Web Search](#) - [hep.princeton.edu](#) - [www-tfp.physik.uni-karlsruhe.de](#) - [pi1.physi.uni-heidelberg.de](#) - [all 6 versions »](#)

### Ab initio calculations of the lattice dynamics of boron nitride nanotubes

L Wirtz, A Rubio, RA de la Concha, A Loiseau - Physical Review B, 2003 - [link.aps.org](#)

... Therefore, as a first **check** on the frequencies of active ... groups have been used to evaluate the section **rules** for the ... 7~al# which are related to the **optical** out-of ...

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CA Mack - FINLE Technologies (Austin, TX: 1997)

[Cited by 12 - Web Search](#)**Three-dimensional simulation of optical lithography**KK Toh, AR Neureuther - Proc. SPIE, 1991 - [adsabs.harvard.edu](#)

Title: Three-dimensional simulation of optical lithography Authors: Toh,

Kenny K.; Neureuther, Andrew R. Affiliation: AA(Univ. of ...)

[Cited by 8 - Web Search](#)**Efficient and rigorous three-dimensional model for optical lithography simulation**KD Lucas, H Tanabe, AJ Strojwas - J. Opt. Soc. Am. A, 1996 - [josaa.osa.org](#)

... for optical lithography simulation ... 6,7 This new model is ideally suited to the

simulation of 3-D optical lithography processing problems. ...

[Cited by 4 - Web Search](#) - [josaadev.osa.org](#) - [josaa.osa.org](#) - [adsabs.harvard.edu](#)**Impact of lens aberrations on optical lithography**T Brunner - IBM Journal of Research and Development, 1997 - [research.ibm.com](#)... simulated by the PROLITH/2\* simulation program<sup>2</sup> under ... three-leaf-clover aberration

on lithography is to ... a few nm precision by modern optical overlay metrology ...

[Cited by 23 - Cached - Web Search](#) - [research.ibm.com](#) - [portal.acm.org](#) - [csa.com](#)**Spatial filtering for depth of focus and resolution enhancement in optical lithography**H Fukuda, T Terasawa, S Okazaki - J. Vac. Sci. Technol. B, 1991 - [link.aip.org](#)

... This enhances depth of focus while maintaining high resolution capability in optical

lithography. ... Simulation and modeling of fabrication processes.

[Cited by 11 - Web Search](#) - [adsabs.harvard.edu](#)**Resolution Enhancement Techniques in Optical Lithography**K Ronse, L Van - [fabtech.org](#)

... Figure 2 Lumped parameter model simulation illustrating the improvement in DOF ... Figure

4 (above) The optical lithography roadmap, detailed with the various ...

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... in a half-micron optical lithography by the focus latitude enhancement exposure method:

**Simulation ...**H Fukuda, N Hasegawa, S Okazaki - Journal of Vacuum Science & Technology B: Microelectronics ..., 1989 - [dx.doi.org](#)

&gt;/&gt; Improvement of defocus tolerance in a half-micron optical lithography by the focus latitude enhancement exposure method: Simulation and experiment. ...

[Cited by 5 - Web Search](#) - [link.aip.org](#) - [adsabs.harvard.edu](#)**Comparison of recent development models in optical lithography simulation**GG Arthur, C Wallace, B Martin - Proc. SPIE, 1998 - [adsabs.harvard.edu](#)

Title: Comparison of recent development models in optical lithography simulation

Authors: Arthur, Graham G.; Wallace, Christine; Martin, Brian Affiliation: AA ...

[Cited by 3 - Web Search](#) - [link.aip.org](#)

**Simulation of optical lithography**

A Erdmann, W Henke - Proceedings of SPIE, 2003 - adsabs.harvard.edu

Title: **Simulation of optical lithography** Authors: Erdmann, Andreas; Henke, Wolfgang

Affiliation: AA(Fraunhofer Institute for Silicon Technology) Journal: Proc. ...

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C Mack - Inc.(1997)

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Subwavelength **optical lithography**: challenges and impact on physical design

AB Kahng, YC Pati - ISPD, 1999 - portal.acm.org

... essential com- panion to the "**checking-centric**" mindset ... the context of subwavelength

**optical lithography**, the above ... and PSM-related design **rules** will move ...

Cited by 14 - [Web Search](#) - portal.acm.org

Resolution Enhancement Techniques in **Optical Lithography**, It's not just a Mask Problem

LW Liebmann - ... and Next-Generation **Lithography** Mask Technology VIII, Proc. ... - eecs.umich.edu

... Absent from Table 1 is **optical** proximity correction, customarily ... have to be optimized

experimentally or through **simulation** by the **lithography** groups and ...

Cited by 3 - [View as HTML](#) - [Web Search](#) - adsabs.harvard.edu - link.aip.org

... Phase Shifted Mask Designs for a Full Logic Gate Level: Design **Rules** and Design Rule **Checking**

L Liebmann, J Lund, FL Heng, I Graur - DAC, 2001 - portal.acm.org

... the lifetime of a given generation of **optical lithography** tools. ... **rules** are derived

from the **lithography** system in ... One could use a **simulation**-based method which ...

Cited by 6 - [Web Search](#) - ieexplore.ieee.org - videos.dac.com - hwswworld.com - all 12 versions »

Practical applications of 2-D **optical** proximity corrections for enhanced performance of 0.25 $\mu$  m ...

H Chuang, P Gilbert, W Grobman, M Kling, K Lucas, ... - Electron Devices Meeting, 1997. Technical Digest., ..., 1997 - ieexplore.ieee.org

... an interactive cycle involving **optical** modeling, OPC ... could be achieved using these

tuned **lithography** simulations in ... Accurate tuning of the **simulation** models is ...

Cited by 2 - [Web Search](#) - io.com - ieexplore.ieee.org

Impact of RET on physical layouts:

FM Schellenberg, L Capodieci - ISPD, 2001 - portal.acm.org

... concerns techniques known as OPC (**Optical** & Process ... is a physical modification to

the **lithography** tool, and ... understood, and can be modeled through **simulation**. ...

Cited by 2 - [Web Search](#) - acm.org - sigda.org - portal.acm.org

Model-based OPC/DRC considering local flare effects

H Futatsuya, T Yao, M Osawa, K Ogino, H Hoshino, H ... - Proceedings of SPIE, 2004 - link.aip.org

... manufacturing IC devices that use **lithography** generations of ... simply by the sum of

**optical** intensity and ... impact of local flare, the **simulation** model including ...

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Sub-Wavelength **Lithography** Using OPC

FM Schellenberg - fabtech.org

... Both **rules**- based corrections, for simple improvements, and model ... example, all papers

in Session 5: **Lithography Simulation**, in **Optical/Laser Microlithography** ...

[Web Search](#) - semiconductorfabtech.com - eecs.umich.edu - semiconductorfabtech.com

Silicon-Level Physical Verification of Sub Wavelength (tm) Designs

FC Chang, M Kwok, K Rachlin, R Pack, NT Inc, CA ... - Proceedings of the 12th International Conference on VLSI ..., 1999 - doi.ieeecomputersociety.org

... with a set of manufacturing process **rules** such as the ... this by using very fast

**lithography simulation** to produce ... using Practical 2-D **Optical Proximity Correction** ...

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**A Fast Lithography Verification Framework for Litho-Friendly Layout Design**

YC Ban, SH Choi, KH Lee, DH Kim - [doi.ieeecomputersociety.org](#)

... Kim, M. Yoo, J. Kong, "**Simulation**-based critical ... friendly layout design for low **lithography**", Proc ... Resolution enhancement techniques in **optical lithography**, 2001 ...

[Web Search](#)

**Optical proximity correction (OPC): friendly maze routing**

MDF Wong - Proceedings of the 41st annual conference on Design ..., 2004 - [portal.acm.org](#)

... The distortions in opti- cal **lithography** include corner ... The design rules basically capture the first order ... is different from the **optical simulation** grid size. ...

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### Future Fab Intl.

This has sometimes been called an **ORC**, for **Optical Rules Check**, ... The resulting field dependent aberrations can be used in the **simulation** algorithms that ...

[www.future-fab.com/documents.asp?grID=213&d\\_ID=1202](http://www.future-fab.com/documents.asp?grID=213&d_ID=1202) - 92k - [Cached](#) - [Similar pages](#)

### Optimal insertion points for OPC and PSM in design flows

... the introduction of the "OPC DRC" step (more commonly called **ORC**, **optical rules check**) ensures that OPC changes are actually manufacturable, ...

[www.mentor.com/products/ic\\_nanometer\\_design/news/articles/opc\\_psm\\_design\\_flows.cfm](http://www.mentor.com/products/ic_nanometer_design/news/articles/opc_psm_design_flows.cfm) - 32k - [Cached](#) - [Similar pages](#)

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Calibre **ORC** (**Optical** and Process. Rule Checking) provides full-chip ... DRC".

The **simulation** is based on the. **optical** model and process model ...

[www.mentor.com/.../calibre\\_ret/loader.cfm?url=/commonspot/security/getfile.cfm&pageid=9969](http://www.mentor.com/.../calibre_ret/loader.cfm?url=/commonspot/security/getfile.cfm&pageid=9969) -

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generated by CMP **simulation**. The wafer topography variations result in local ...

OPC and **optical** rule checking (**ORC**). TOPC is performed based on the DMLs. ...

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Weak points are collected through the **optical**. rule checking (**ORC**), which uses fast and accurate. **simulation** of the aerial image and resist image at the ...

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to some highly constrained design **rules** for these cases [5]. ... process **simulation**, such as Calibre **ORC**, the wafer image itself ...

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... by changing aperture sizes and shapes (**optical** and process ... designed layout and a DRC **check** of the ... generated, and then checked using conventional design **rules**. ...

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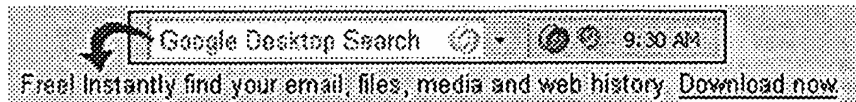
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... One potential problem with using the Skirmish Rules with the Random ...

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says Thomas Blaesi, vice president marketing and business development. ...

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and resist image at the. wafer level. The parameters for CAE are exposure ...

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are the full-chip solution to accurate silicon-versus-layout ...

[www.spie.org/app/exhibition/index.cfm?exhibitor\\_id=5666&fuseaction=exhibitor\\_detail&meeting\\_id=58](http://www.spie.org/app/exhibition/index.cfm?exhibitor_id=5666&fuseaction=exhibitor_detail&meeting_id=58) - 36k -[Cached](#) - [Similar pages](#)Semiconductor International - Effecting Mask Costs by Solving the ...

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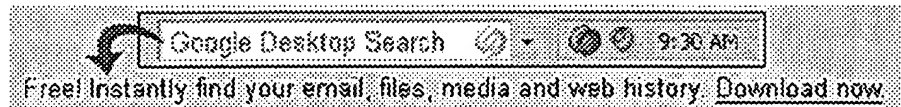
UETA and the subsequent administrative **rule** apply only to electronic records ...

Public records under **ORC** 149.43 are any record that is kept by any public ...

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### DRC FAQs

Which command files (DRC/LVS/LPE) and their corresponding EDA tools are ...  
yield and avoid potential problems caused by possible **layout rule violations**. ...  
[www.umc.com/English/design/h\\_1.asp](http://www.umc.com/English/design/h_1.asp) - 81k - [Cached](#) - [Similar pages](#)

### IC Station Tutorial

... individual **layout** blocks, both using DRC and LVS, the purpose of running LVS  
now is ... This can cause design **rule violations** in the top-level **layout**, ...  
[www.cs.wisc.edu/~david/courses/cs755/cs755/tutorials/tutorial8/tutorial8.html](http://www.cs.wisc.edu/~david/courses/cs755/cs755/tutorials/tutorial8/tutorial8.html) - 10k - [Cached](#) - [Similar pages](#)

### [PDF] Design Migration flyer 0146-1

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necessary documents, DRC (Design Rule Check), LVS (Layout versus Schematic) ...  
the DIVA DRC and also LVS violations. The DIVA rules file replicates the ...  
[www.arm.com/pdfs/146-1%20Design%20Migration.pdf](http://www.arm.com/pdfs/146-1%20Design%20Migration.pdf) - [Similar pages](#)

### [doc] Tips on DRC and LVS (Micro—Magic)

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DRC: 1. Continuous Design-Rule Checking. When you are editing a **layout** with Magic,  
... LVS. Make sure your **layout** design is DRC clean; Save all cellviews. ...  
[bwrc.eecs.berkeley.edu/Classes/ICDesign/EE141\\_f03/CadenceLabs/Tips\\_DRC\\_LVS\\_Magic.doc](http://bwrc.eecs.berkeley.edu/Classes/ICDesign/EE141_f03/CadenceLabs/Tips_DRC_LVS_Magic.doc) - Jul 10, 2005 -  
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### :: SMIC :: Design Service

Calibre DRC/LVS and xRC provide the physical verification and extraction solution  
... **rule checking (DRC)**, **layout** vs. schematic (LVS), silicon vs. **layout**, ...  
[www.smics.com/website/enVersion/DS/SMIC-Mentor\\_Graphics\\_Reference\\_Flow\\_1.0.htm](http://www.smics.com/website/enVersion/DS/SMIC-Mentor_Graphics_Reference_Flow_1.0.htm) - 21k -  
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Intelligent **layout** automation in CosmosLE results in LVS- and DRCcorrect cell and  
... awareness to prevent design-rule violations during place and route. ...  
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connectivity and verifying the **layout** against the schematic(LVS) ... reliably and  
repeatably. DRC checks to see if your **layout** violate any of these **rules**. ...  
[www.cadence.ncsu.edu/NCSUCadenceTutorial/LayoutTutorial.pdf](http://www.cadence.ncsu.edu/NCSUCadenceTutorial/LayoutTutorial.pdf) - [Similar pages](#)

### HJTC

HJTC's Customer Design Support Department (CDS), provides DRC, LVS and LPE ...  
yield and avoid potential problems caused by possible **layout rule violations**. ...  
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Cadence Tutorial B: **Layout, DRC, Extraction, and LVS**. 11. Design Rule Checking  
... design rule violations. In future layouts, run DRC frequently as you add ...  
[www-ee.uta.edu/online/jung/EE5319/pdfs/Layout\\_sim1.pdf](http://www-ee.uta.edu/online/jung/EE5319/pdfs/Layout_sim1.pdf) - [Similar pages](#)

**EE4321-VLSI CIRCUITS : Cadence' Virtuoso Layout Information**  
**LVS (layout versus Schematic)** is another important verification. While **DRC** just  
checks if your layout follows the rules set by a technology, ...  
[www.cisl.columbia.edu/grads/sumit/drc\\_lvs.html](http://www.cisl.columbia.edu/grads/sumit/drc_lvs.html) - 6k - [Cached](#) - [Similar pages](#)

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You learn to **design** a relational **database** using data modelling and normalisation, ... Modelling in analysis and **design**; Focusing on business **rules** ...  
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### SSW Rules to Better SQL Server Databases

Frequently when I'm reviewing a clients SQL Server **database design**, the in-house ... We have a program called SSW SQL Auditor to **check** for this **rule**: ...  
[www.ssw.com.au/SSW/Standards/Rules/RulestoBetterSQLServerDatabases.aspx](http://www.ssw.com.au/SSW/Standards/Rules/RulestoBetterSQLServerDatabases.aspx) - 101k - Jul 10, 2005 - [Cached](#) - [Similar pages](#)

### Database Design Guide

Most probably these Dos and Don'ts of **database design** will reduce your efforts and help you to ... There are other advantages of consistent naming **rules**. ...  
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### Components in Electronics - CIE

Is a single **database** really necessary for a chip **design** tool? ... Verification and test data can then used for **design rule checking** throughout the ...  
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### Database Programming & Design July 1998 Product News

Logic Works' **database design** tool opens up this month's products ... •Advantage Environment **Check** Utility, which lets users run a diagnostic **check** on their ...  
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### SQL Server Reference Guide

In the last several articles, we've learned to develop a **database design** in ... The logical model we have largely fits this **rule**, so the first part of the ...  
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### SQL Server Database Design Performance Tuning Tips

As a **rule** of thumb, **design** your **database** to minimize potential user contention. ... The Query Optimizer can use **check** constraints to help speed up query ...  
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### Database Design Methodology Summary

This page gives a summary of the **Database Design** Methodology for Relational **Databases** and ... **Design** the enterprise constraint **rules** for the target DBMS. ...  
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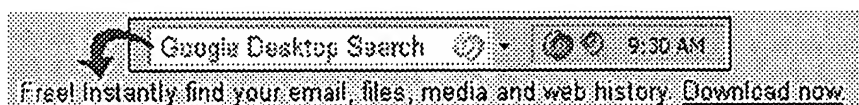
List each of Codd's **rules** and discuss any implications for **database** ... Can act as a **cross-check** to ensure that a **database. design** is complete by allowing ...

[www.utexas.edu/academic/cit/howto/resources/database/relational.answers.pdf](http://www.utexas.edu/academic/cit/howto/resources/database/relational.answers.pdf) -

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Vector DRC uses the **Gerber description** of the position, size and shape of elements to determine clearance and contact between elements. ...

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### Generating Gerber Data

For a detailed **description** of the Gerber RS-274X format, see here ... This list is included in the Gerber files and will be used by the Laser Photoplotter ...

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### D-codes, Apertures and Gerber Plot Files

Gerber photoplotters can draw arcs when instructed to do so. ... This is the **description** of what is contained in each aperture position. ...

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Richard Gerber Personal Webpage: Field Committee: Achievements – Ph.D.: University of Pennsylvania, 1991 – Asst Professor, 1991-2001, ...

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**Calibre** physical verification tool suite, **Calibre DRC** and **Calibre LVS**, ensures that. IC physical designs conform to foundry manufacturing rules and ...

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[www.europactice.imec.be/europactice/on-line-docs/prototyping/ti/doc\\_UMC25\\_mixed.html](http://www.europactice.imec.be/europactice/on-line-docs/prototyping/ti/doc_UMC25_mixed.html) - 12k -

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spice model; LO25\_33V\_noise\_ver21.pdf - Noise results ...

[www.europactice.imec.be/europactice/on-line-docs/prototyping/ti/doc\\_VST\\_UMC25\\_logic.html](http://www.europactice.imec.be/europactice/on-line-docs/prototyping/ti/doc_VST_UMC25_logic.html) - 11k

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4. When you are done building the inverter, build a ring oscillator circuit ...

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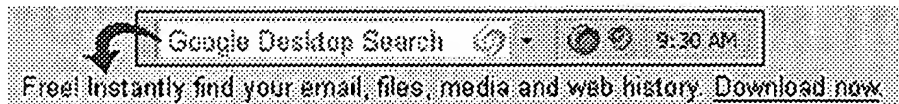
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The techniques of Mask **Rule Checking** (MRC) and Optical **Rule Checking** (ORC) ...  
To address this issue, a technique known as Critical Failure **ORC** (CFORC) was ...  
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Calibre **ORC** (Optical and Process. **Rule Checking**) provides full-chip ...

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... their designs and OPC and **ORC** (optical-**rule-checking**) tools are process-accurate,  
says Thomas Blaesi, vice president marketing and business development. ...  
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The combined team has also created two new products for optical-process **rule**  
**checking** called Calibre **ORC** and Calibre **ORC-reporter**, available now, ...  
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**rule checking** (**ORC**), which uses fast and accurate. simulation of the aerial image  
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are the full-chip solution to accurate silicon-versus-layout ...

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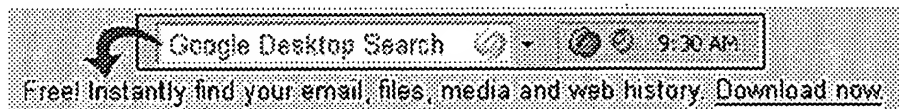
UETA and the subsequent administrative rule apply only to electronic records ...

Public records under ORC 149.43 are any record that is kept by any public ...

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#### Future Fab Intl.

This has sometimes been called an **ORC**, for **Optical Rules Check**, because distortions

... Sharing this **database** with OPC and PSM can lead to both intrinsic ...

[www.future-fab.com/documents.asp?grID=213&d\\_ID=1202](http://www.future-fab.com/documents.asp?grID=213&d_ID=1202) - 92k - [Cached](#) - [Similar pages](#)

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... insertion but also in the **optical rules** checking (**ORC**) step that checks ...

OPC and **optical** rule checking (**ORC**). TOPC is performed based on the DMLs. ...

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Calibre **ORC** (**Optical** and **Process**. Rule Checking) provides full-chip ... **ORC** and

print-image verification. tools **check** for unintended side- ...

[www.mentor.com/.../calibre\\_ret/loader.cfm?url=/commonspot/security/getfile.cfm&pageid=9969](http://www.mentor.com/.../calibre_ret/loader.cfm?url=/commonspot/security/getfile.cfm&pageid=9969) - [Similar pages](#)

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and **optical** and process correction (OPC) to the mask data format conver- ...

**check** of the mask making **rules**. based on a flexible, programmable. **rules** deck ...

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... 1:55 pm: Advanced manufacturing **rules** **check** (MRC) for fully-automated ...

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Operating system support for **ORC** and real-time object request brokers \* **Database**

architectures for **ORC** \* Real-time simulation \* Testing, verification, ...

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**ORC** Begins Issuing DoD External Certification Authority Certificates ...

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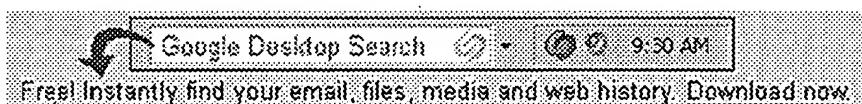
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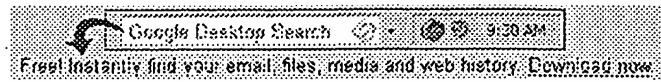
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